October 1, 2014

08:00-9:00 — Registration

09:00-09:15 — Conference Opening

S. Hamdioui, M.Ottavi General Chairs
S. Kundu, S. Pontarelli Program Chairs

09:15-10:00 — Keynote Talk

Josep Torrellas, Univ. of Illinois -- Urbana-Champaign
Tackling Parameter Variation from an Architectural Perspective

10:00-10:20 — Coffee Break

10:20-11:20 — Session 1: Memories

Session Chair: Cecilia Metra, University of Bologna

O1.1 Triggering Trojans in SRAM Circuits with X-Propagation
Senwen Kan and Jennifer Dworak

O1.2 Characterization of Data Retention Faults in DRAM Devices
Angelo Bacchini, Marco Rovatti, Gianluca Furano and Marco Ottavi

O1.3 *Characterizing Soft Error Vulnerability of* Cache Coherence Protocols for Chip-Multiprocessors
Chuanlei Zheng and Shuai Wang

11:20-11:30 — Short break

11:30-12:30 — Session 2: Self Testing

Session Chair: Maria Michael, University of Cyprus

O2.1 Power Droop Reduction During Logic BIST of Sequential ICs with Launch-On-Shift Scan
Martin Omana, Daniele Rossi, Edda Beniamino, Cecilia Metra, Chandra Tirumurti and Rajesh Galivanche

O2.2 Diagnostic Self-Test for Dynamically Scheduled Superscalar Processors based on Reconfiguration Techniques for Handling Hard Faults
Mario Schölzel, Tobias Koal and Heinrich T. Vierhaus

O2.3 Exploration of System Availability During Software-Based Self-Testing in Many-core Systems under Test Latency Constraints
Michael Skitsas, Chrysostomos Nicopoulos and Maria Michael

12:30-14:00 — Lunch

14:00-15:20 — Session 3: Security and Fault Tolerance

Session Chair: Prashant Joshi

O3.1 Protecting Cryptographic Hardware against Malicious Attacks by Nonlinear Robust codes
Victor Tomashevich, Yaara Neumeier, Raghavan Kumar, Osnat Keren and Ilia Polian

O3.2 CSST: Preventing Distribution of Unlicensed and Rejected ICs by Untrusted Foundry and Assembly
Md. Tauhidur Rahman, Domenic Forte, Qihang Shi, Gustavo Contreras and Mohammad Tehranipoor

O3.3 *Reusing DfT Infrastructure For Online* Security Monitoring of Systems-on-Chip
Jerry Backer, David Hély and Ramesh Karri

O3.4 Security Methods in Fault Tolerant Modified Line Graph based
Prashant Joshi and Said Hamdioui

15:20-15:50 — Coffee Break & Poster Session I

15:50-17:30 — Session 4: Emerging technologies

Session Chair: Glenn Chapman, Simon Fraser Univ.

O4.1 A System-level Scheme for Resistance Drift Tolerance of a Multilevel Phase Change Memory
Fabrizio Lombardi, Jie Han and Pilin Junsangsri

O4.2 Designs and Analysis of Non-Volatile Memory Cells for Single Event Upset (SEU) Tolerance
Fabrizio Lombardi, Wei Wei and Kazuteru Namba

O4.3 Reliability Estimation at Block-Level Granularity of Spin-Transfer-Torque MRAMs
Marco Indaco, Elena Vatajelu, Stefano Di Carlo, Paolo Prinetto, Rosa Rodriguez-Montanes and Joan Figueras

O4.4 Oxide based Resistive RAM: ON/OFF Resistance Analysis versus Circuit Variability
Hassen Aziza, Haithem Ayari, Santhosh Onkaraiah, Mathieu Moreau, Jean-Michel Portal and Marc Bocquet

O4.5 Using Memristor State Change Behavior to Identify Faults in Photovoltaic Arrays
Jimson Mathew, Yuanfan Yang, Marco Ottavi and Dhiraj K Pradhan

October 2, 2014

08:00-9:00 — Registration

09:00-10:00 — Keynote Talk

Neeraj Suri, TU Darmstadt -- Darmstadt
Quo Vadis Diagnosis: A Systems View

10:00-10:20 — Coffee Break

10:20-11:20 — Session 5: System on Chip

Session Chair: Cristiana Bolchini, Politecnico Milano

O5.1 TSV-to-TSV Inductive Coupling-Aware Coding Scheme for 3D Network-on-Chip
Ashkan Eghbal, Pooria Yaghini, Siavash S. Yazdi and Nader Bagherzadeh

O5.2 Rescuing Healthy Cores Against Disabled Routers
Masoumeh Ebrahimi, Wang Junshi, Letian Huang, Masoud Daneshtalab and Axel Jantsch

O1.3 A Non-minimal Turn Model for Fault Tolerant and Highly Adaptive Routing in 2D NoCs
Manoj Kumar, Vijay Laxmi, Manoj Gaur, Masoud Daneshtalab, Masoumeh Ebrahimi and Mark Zwolinski

11:20-11:30 — Short break

11:30-12:30 — Session 6: Sensors

Session Chair: Fabrizio Lombardi, Northeastern Univ.

O6.1 Performance Sensor for Tolerance and Predictive Detection of Delay-Faults
Jorge Semião, André Romão, David Saraiva, Carlos Leong, Marcelino Santos, Isabel Teixeira and Paulo Teixeira

O6.2 Improved Correction Algorithm for Hot Pixels in Digital Imagers
Glenn Chapman, Rohit Thomas, Rahul Thomas, Israel Koren and Zahava Koren

O6.3 Diagnosis of segment delay defects with current sensing
Wisam Aljubouri, Ahish Somashekar, Themistoklis Haniotakis and Spyros Tragoudas

12:30-14:00 **Lunch**

14:00-15:20 **Session 7: Analysis and Synthesis of resilient systems**

Session Chair: Spyros Tragoudas, Southern Ill. Univ.

O7.1 A Scheduling Algorithm in Datapath Synthesis for Long Duration Transient Fault Tolerance
Tsuyoshi Iwagaki, Tatsuya Nakaso, Ryoko Ohkubo, Hideyuki Ichihara and Tomoo Inoue

O7.2 Artificial Intelligence Based Task Mapping and Pipelined Scheduling for Checkpointing on Real Time Systems with Imperfect Fault Detection
Anup Das, Akash Kumar and Bharadwaj Veeravalli

O7.3 A Probabilistic Analysis of Resilient Reconfigurable Designs
Alirad Malek, Stavros Tzilis, Danish Anis Khan, Ioannis Sourdis, Georgios Smaragdos and Christos Strydis

O7.4 Domino Effect Protection on Dataflow Error Detection and Recovery
Tiago A. O. Alves, Leandro A. J. Marzulo, Sandip Kundu and Felipe M. G. França

15:20-15:50 **Coffee Break & Poster Session II**

15:50-17:30 **Session 8: Fault tolerance in FPGA devices**

Session Chair: Bill Eklow, Cisco Systems.

O8.1 Decreasing FIT with Diverse Triple Modular Redundancy in SRAM-based FPGAs
Lucas Antunes Tambara, Fernanda Kastensmidt, Paolo Rech and Christopher Frost

O8.2 A Fault Injection Methodology and Infrastructure for Fast Single Event Upsets Emulation on Xilinx SRAM-based FPGAs
Stefano Di Carlo, Paolo Prinetto, Daniele Rolfo and Pascal Trotta

O8.3 A Fault Injection Methodology and Design and implementation of a Self-Healing Processor on SRAM-based FPGAs
Alexandros Vavousis, Mihalis Psarakis, Cristiana Bolchini and Antonio Miele

O8.4 *Aging Analysis for Recycled FPGA Detection*
Halit Dogan, Domenic Forte and Mark Tehranipoor

O8.5 *Analytic Reliability Evaluation for Fault-tolerant Circuit Structures on FPGAs*
Jahanzeb Anwer and Marco Platzner

17:30-18:30 **DFT TPC Meeting**

Program of the 17th IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

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