# IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

# October 2-4, 2019, ESA-ESTEC & TU Delft, Netherlands

#### **General co-Chairs**

Marco Ottavi

Università di Roma "Tor Vergata", IT marco.ottavi@uniroma2.it

#### **Antonios Tavoularis**

European Space Agency, NL antonios.tavoularis@esa.int

## **Program co-Chairs**

Vilas Sridharan AMD, USA

vilas.sridharan@amd.com

#### Mihalis Psarakis

University of Piraeus, GR mpsarak@unipi.gr

### **Finance Chair**

Marco Rovatti

European Space Agency, NL

#### **Publicity Chair** Luca Cassano

Politecnico di Milano, IT

#### **Publication Chair**

**Prashant Nair** 

University of British Columbia, CA

#### **Local Arrangements Chair** Gianluca Furano

European Space Agency, NL Alessandra Menicucci

TU Delft, NL

#### **Special Session Chair** Luigi Dilillo LIRMM, FR

### **Technical Program Committee**

- L. Anghel, TIMA, FR
- G. Beltrame, Ecole Polytechinque de Montreal, CA
- E. Bezerra, UFSC, BR
- C. Bolchini, Politecnico di Milano, IT
- L. Cassano, Politecnico di Milano, IT G. Chapman, Simon Fraser University, CA
- L. Dilillo, LIRMM, FR
- S. Eggersglüß, Mentor Graphics, US O. Ergin, TOBB University, TR
- A. Evans, IROC Technologies, FR
- G. Furano, European Space Agency, NL
- D. Gizopoulos, University of Athens, GR
- J. Han, University of Alberta, CA
- D. Hely, Grenoble INP, FR
- C. Huang, National Tsing Hua University, TW H. Ichihara, Hiroshima City University, JP
- V. Izosimov, Semcon AB, SE
- X. Jian, Virginia Tech, US P. Joshi, Intel, US
- N. Karimi, University of Maryland, US
- S. Khursheed, University of Liverpool, UK Y-B Kim, Northeastern University, US
- B. Kruseman, NXP Semiconductors, NL F. Lombardi, Northeastern University, US
- Marinissen, IMEC, BE D. Melo, University of Vale do Itajaí, BR
- A. Menicucci, University of Delft, NL
- M. Michael, University of Cyprus, CY A. Miele, Politecnico di Milano, IT
- M. Kermani, University of South Florida, US
- P. Nair, University of British Columbia, CA K. Namba, Chiba University, JP
- N. Nicolici, McMaster University, CA
- C. Nicopoulos, University of Cyprus, CY M. Ottavi, University of Rome Tor Vergata, IT
- I. Polian, University of Stuttgart, DE
- M. Psarakis, University of Piraeus, GR A. Rahmani, UC Irvine, US and TU Wien, AT P. Rech. UFRGS. BR
- P. Revriiego, Universidad Carlos III de Madrid, ES
- D. Rossi, University of Hertfordshire, UK M. Rovatti, European Space Agency, NL
- Sandionigi, CEA, FR
- R. Shafik, School of EEE, Newcastle University, UK M. Shafique, Vienna University of Technology, AT
- Siddiqua, AMD, US
- I. Sourdis, Chalmers University of Technology, SE V. Sridharan, AMD, US
- M. Taouil, Delft University of Technology, NL
- A. Tavoularis, European Space Agency, NL
- Teixeira, IST/INESC-ID, PT
- N. Touba, The University of Texas at Austin, US S. Tragoudas, Southern Illinois University, US
- B. Venu, ARM Ltd, UK
- Q. Xu, The Chinese University of Hong Kong, HK Yalcin, Abdullah Gul University, TR
- T. Yoneda, Tokyo Institute of Technology, JP

# **Call for Papers**

DFT is an annual Symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test. reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following:

- 1. Yield Analysis and Modeling: Defect/fault analysis and models; statistical yield modeling; diagnosis; critical area and other metrics.
- 2. Testing Techniques: Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; online testing; signal and clock integrity.
- 3. Design for Testability in IC Design: FPGA, SoC, NoC, ASIC, low power design and microprocessors.
- 4. Error Detection, Correction, and Recovery: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques; architectural and system-level techniques.
- 5. Dependability Analysis and Validation: Fault injection techniques and frameworks; dependability and characterization.
- 6. Repair, Restructuring and Reconfiguration: Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing; reliable FPGA-based systems.

- 7. Defect and Fault Tolerance: Reliable circuit/system synthesis; fault tolerant processes and design; design space exploration for dependable systems, transient/soft faults.
- 8. Radiation effects: SEEs on nanotechnologies; modeling of radiation environments; radiation experiments: radiation hardening techniques.
- 9. Aging and Lifetime Reliability: Aging characterization and modeling; design and run-time reliability, thermal, and variability management and recovery.
- 10. Dependable Applications and Case Studies: Methodologies and case studies for IoTs, automotive, rail-way, avionics and space, autonomous systems, industrial control, etc.
- 11. Emerging Technologies: Techniques for 2.5D/3D ICs, quantum computing architecttures, memristors, spintronics, microfluidics, etc. 12. Design for Security: Fault attacks, fault tolerance-based countermeasures, scan-based

attacks and countermeasures, hardware troians.

security vs. reliability trade-offs, interaction between VLSI test, trust, and reliability. Paper Submission: Prospective authors are invited to submit original and unpublished contributions. Two types of submissions are possible: (i) regular papers (6 pages), and (ii) short papers (4 pages). Both types will be included in the symposium proceedings and should adhere to the IEEE conference

electronically. Please refer to the symposium web page for updated information. Call for Special Sessions: Proposals for Special Sessions are also invited. For more information, visit symposium website and see the specific call.

template, 2-columns style (available on conference web site), and submitted as a PDF file,

Paper Publication: Only original, unpublished work will be accepted, for regular or short presentation at the symposium. Proceedings will be published by the IEEE Computer Society and will appear in the Digital Library. All papers will be considered for the DFT 2019 Best Paper Award. Furthermore, selected papers will be considered for a special issue/section of an archival journal.

Author Registration: Every accepted paper MUST have at least one full paid registration by the time the camera-ready paper is submitted for inclusion in the proceedings, and one of the authors is expected to attend the Symposium and present the paper.

Venue: The symposium is going to Europe for its 32nd edition and will be co-hosted by the Space Research and Technology Centre of the European Space Agency (ESA-ESTEC) and TU Delft, Netherlands. The first two days of the symposium will be held at ESA-ESTEC and the 3rd day will be held at TU Delft. The city of Leiden - which is between the two sites - is conveniently located close to Amsterdam International Airport and is connected by excellent rail and bus services to both sites.

Prospective authors should adhere to the following deadlines:

Abstract submission: May 3, 2019 **Full paper submissions** May 17, 2019 Notification of acceptance: July 12, 2019 Camera ready and author's registration: August 9, 2019

Sponsored by:







Computer