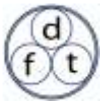

IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

October 19-21, 2020, ESA-ESRIN, Italy

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Call for Papers

***Message re. COVID-19:** In view of the unprecedented COVID-19 situation, the DFT 2020 organizing committee is still committed to preserve the event as scheduled, keeping in mind the importance of DFT symposium for the community. We encourage prospective contributors to submit their work to the symposium considering that it will take place normally. However, we are ready to put in place the following mitigation measures depending upon circumstances:*

- *relax attendee cancellation and refund policies.*
- *provide author(s) and keynote presenter(s), who are be impacted, options for virtual presentation.*
- *allow for publication despite the inability of authors to present their accepted paper.*

The organizing committee will keep prospective authors updated for any of the above mitigation measures.

DFT is an annual Symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following:

1. Yield Analysis and Modeling: Defect/fault analysis and models; statistical yield modeling; diagnosis; critical area and other metrics.
2. Testing Techniques: Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; online testing; signal and clock integrity.
3. Design for Testability in IC Design: FPGA, SoC, NoC, ASIC, low power design and micro-processors.
4. Error Detection, Correction, and Recovery: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques; architectural and system-level techniques.
5. Dependability Analysis and Validation: Fault injection techniques and frameworks; dependability and characterization.
6. Repair, Restructuring and Reconfiguration: Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing; reliable FPGA systems.
7. Defect and Fault Tolerance: Reliable circuit/system synthesis; fault tolerant processes and design; design space exploration for dependable systems, transient/soft faults.
8. Radiation effects: SEEs on nanotechnologies; modeling of radiation environments; radiation experiments; radiation hardening techniques.
9. Aging and Lifetime Reliability: Aging characterization and modeling; design and run-time reliability, thermal, and variability management and recovery.
10. Dependable Applications and Case Studies: Methodologies and case studies for IoTs, automotive, rail-way, avionics and space, autonomous systems, industrial control, etc.
11. Emerging Technologies: Techniques for 2.5D/3D ICs, quantum computing architectures, memristors, spintronics, microfluidics, etc.
12. Design for Security: Fault attacks, fault tolerance-based countermeasures, scan-based attacks and countermeasures, hardware trojans, security vs. reliability, interaction between VLSI test, trust, and reliability.

Paper Submission: Prospective authors are invited to submit original and unpublished contributions in the areas described above. Submitted papers should be no longer than 6 pages and adhere to the IEEE conference template, 2-columns style (available on conference web site). Papers can be accepted as regular papers (oral presentations) or posters. Both types will be included in the IEEE proceedings; the page limit for proceedings is 6 pages for regular papers and 4 pages for posters. Please refer to the symposium web page for updated information.

Call for Special Sessions: Proposals for Special Sessions are also invited. For more information, visit symposium website and see the specific call.

Paper Publication: Only original, unpublished work will be accepted, for oral or poster presentation at the symposium. Proceedings will be published by the *IEEE Computer Society* and will appear in the *Digital Library*. All papers will be considered for the *DFT 2020 Best Paper Award*. Furthermore, selected papers will be considered for a special issue/section of an archival journal.

Author Registration: Every accepted paper MUST have at least one *full* paid registration by the time the camera-ready paper is submitted for inclusion in the proceedings, and one of the authors is expected to attend the Symposium and present the paper.

Venue: The symposium in its 33rd edition will be supported for a second consecutive year by the European Space Agency (ESA) and will take place at the ESA's establishment in Italy, ESA-ESRIN. ESA-ESRIN is the European centre of excellence for exploitation of Earth observation missions. ESRIN is located in Frascati, a small town close to Rome, which is well-connected by train services with the Rome central station and the Fiumicino International Airport.

Prospective authors should adhere to the following deadlines:

Full paper submissions: ~~May 22, 2020~~ **June 5, 2020**
Notification of acceptance: ~~July 3, 2020~~ **July 10, 2020**
Camera ready and author's registration: July 31, 2020

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