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Defect and Fault Tolerance in VLSI and Nanotechnology Systems
Elsevier Journal of Microelectronics Reliability
http://www.dfts.org/specialissue.htm

Scope: The production of highly reliable and secure electronic devices and systems represents a major technological and research challenge together with the increasing demand for matching high computing performance and low power consumption. Latest projections forecast among others, the introduction of new technologies to support emerging applications such as smart diagnostics and healing in healthcare, autonomous driving in automotive that require high safety and quality standards aiming at 0 defective parts per million manufactured parts. In addition, advanced computer systems built with new paradigms like neuromorphic and quantum computing, on one hand promise to achieve better services and more diversified functionalities on the other hand require new approaches for testing and validation. This special issue targets at novel contributions on the topics of reliability in the design, technology and testing of electronic devices and systems, integrated circuit, printed modules, as well as methodologies and tools used for reliability prediction, verification and design validation.

Authors are invited to submit a manuscript to the special section on Defect and Fault Tolerance in VLSI and Nanotechnology Systems. Relevant topics of interest to this special section include (but are not limited to) reliability and dependability-aware analysis and design methodologies:

1. **Yield Analysis and Modeling**: Defect/fault analysis and models; statistical yield modeling; diagnosis; critical area and other metrics.
2. **Testing Techniques**: Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; online testing; signal and clock integrity.
3. **Design for Testability in IC Design**: FPGA, SoC, NoC, ASIC, low power design and microprocessors.
4. **Error Detection, Correction, and Recovery**: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; HW/SW techniques; architectural and system-level techniques.
5. **Dependability Analysis and Validation**: Fault injection techniques and frameworks; dependability and characterization, cross-layer reliability analysis, dependability analysis for AI.
6. **Repair, Restructuring and Reconfiguration**: Repairable logic; reconfigurable circuit design; DFT for online operation; self-healing; reliable FPGA systems.
7. **Radiation effects**: SEEs on nanotechnologies; modeling of radiation environments; radiation experiments; radiation hardening techniques.
8. **Defect and Fault Tolerance**: Reliable circuit/system synthesis; fault tolerant processes and design; design space exploration for dependable systems, transient/soft faults.
9. **Aging and Lifetime Reliability**: Aging characterization and modeling; design and runtime reliability, thermal, and variability management and recovery.
10. **Dependable Applications and Case Studies**: Methodologies and case studies for IoTs, automotive, railway, avionics and space, autonomous systems, industrial control, failsafe systems, dependable AI, etc.
11. **Emerging Technologies**: Techniques for 2.5D/3D ICs, quantum computing architectures, memristors, spintronics, microfluidics, approximate computing, etc.
12. **Design for Security**: Fault attacks, fault tolerance-based countermeasures, scan-based attacks and countermeasures, hardware trojans, system obfuscation and logic locking, secure AI, security vs. reliability, interaction between VLSI test, trust, and reliability.

Submitted papers must include new significant research-based technical contributions in the scope of the journal. Papers under review elsewhere are not acceptable for submission. Extended versions of published conference papers (to be included as part of the submission together with a summary of differences) are welcome, but there must have at least 30% new impacting technical/scientific material in the submitted journal version and there should be less than 50% verbatim similarity level as reported by a tool (such as CrossRef).

How to submit: Please, submit your paper to Elsevier Microelectronics Reliability at https://www.journals.elsevier.com/microelectronics-reliability. Please, select 'DFTS_2021' when you reach the “Article Type” step in the submission process.

Please note the following important dates.

- **Submission Deadline**: April 30, 2022
- **Reviews Completed**: July 18, 2022
- **Major Revisions Due**: September 21, 2022
- **Reviews of Revisions Completed**: December 20, 2022
- **Notification of Final Acceptance**: January 20, 2022

Please address all other correspondence regarding this special issue/section to Lead Guest Editor.

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