



SEPTEMBER 26 (Wed.)

7:30 – 9:00 Registration

9:00 – 9:20 Opening Session

9:20 – 10:40 Session 1 – Fault Injection and Reliability Analysis

Session Chair: Raoul Velazco
(TIMA Laboratory)

FLIPPER: A Flexible Platform for Evaluating Single Event Upset Mitigation Schemes for SRAM based FPGAs

Monica ALDERIGHI, Fabio CASINI, Sergio D'ANGELO, Marcello MANCINI, Giacomo SECHI (INAF), Sandro PASTORE (Sanitas EG), Roland WEIGAND (ESA/ES-TEC)

A Functional Verification based Fault Injection Environment

Alberto BOSIO (LIRMM), Stefano DI CARLO, Alfredo BENSO (Politecnico di Torino), Riccardo MARIANI (YOGITECH SpA)

Comparing fail-safe microcontroller architectures in light of IEC 61508

Riccardo MARIANI (YOGITECH SpA), Peter FUHRMANN (Philips Research Europe)

A Framework for Reliability Assessment and Enhancement in Multi-Processor Systems-On-Chip

Giovanni BELTRAME (European Space Agency), Cristiana BOLCHINI, Antonio MIELE, Luca FOSSATI, Donatella SCIUTO (Politecnico di Milano)

10:40 – 11:00 Coffee break

11:00 – 12:20 Session 2 – Single Event Effects

Session Chair: Hideo Ito
(Chiba University)

Estimating Error Propagation Probabilities with Bounded Variances

Andrea MANUZZATO, Paolo RECH, Simone Mehdi TAHOORI, Hossein ASADI (Northeastern University), Chandra Tirumurti (Intel Corporation)

A Refined Electrical Model for Particle Strikes and its Impact on SEU Prediction

Sybille HELLEBRAND (University of Paderborn), Christian ZOELLIN (Universitaet Stuttgart), Hans-Joachim WUNDERLICH (Universitaet Stuttgart), Bernd STRAUBE (Fraunhofer Inst. für Int. Schaltungen), Thorsten COYM (Fraunhofer IIS-EAS Dresden), Stefan LUDWIG (Fraunhofer Paderborn)

Estimation of Electromigration-Agravating Narrow Interconnects Using a Layout Sensitivity Model
Rani Abou GHALDA, Payman ZARKESH-HA (University of New Mexico)

SET emulation under a quantized delay model
Mario GARCIA VALDERAS, Raul FERNANDEZ CARDENAL, Celia LOPEZ ONGIL, Marta PORTELA-GARCIA, Luis ENTRENA (Universidad Carlos III)

12:20 – 13:30 Lunch

13:30 – 14:50 Session 3 – Reliable NoCs and SoCs

Session Chair: Donatella Sciuto
(Politecnico di Milano)

Reliable Network-on-Chip Using a Low Cost Unequal Error Protection Code

Avijit DUTTA, Nur TOUBA (University of Texas at Austin)

Fault Tolerant Source Routing for Network-on-Chip

Yong-Bin KIM, Young Bok KIM (Northeastern University)

Online NoC Switch Fault Detection and Diagnosis Using a High Level Fault Mode

Armin ALAGHI, Naghmeah KARIMI, Mahshid SEDGHI (University of Tehran), Zainalabedin NAVABI (North-eastern University)

Fault Tolerant SoC Architecture Design for JPEG2000 using Partial Reconfigurability

Abderrahim DOUMAR (University of Technology of Troyes), Kentaroh KATOH, Hideo ITO (Chiba University), Nawal HAMANE (LeadTechDesign)

14:50 – 15:10 Coffee break

15:10 – 16:10 Session 1 – Defect and Fault Tolerance (1)

Session Chair: Luis Entrena
(Universidad Carlos III)

Sensitivity of TMR-hardened circuits to multiple SEUs induced by alpha particles in commercial SRAM-based FPGAs

Andrea MANUZZATO, Paolo RECH, Simone GERARDIN, Alessandro PACCAGNELLA (University of Padova), Luca STERPONE, Massimo VIOLANTE (Politecnico di Torino)

TMR and Partial Dynamic Reconfiguration to mitigate SEU faults in FPGAs

Cristiana BOLCHINI, Antonio MIELE, Marco D. SANTAMBROGIO (Politecnico di Milano)



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Optimization of Self Checking FIR filters by means of Fault Injection Analysis

Salvatore PONTARELLI (University of Rome Tor Vergata), Luca STERPONE (Politecnico di Torino), Gian Carlo CARDARILLI, Marco RE (University of Rome Tor Vergata), Matteo SONZA REORDA (Politecnico Di Torino), Adelio SALSANO (University of Rome Tor Vergata)

16:10 – 16:20 Short break

16:20 – 18:20 Interactive poster presentation

Session Chair: Salvatore Pontarelli
(Università di Roma, "Tor Vergata")

A Defect-Tolerant Molecular-Based Memory Architecture

Yoon-Hwa CHOI, Myeong-Hyeon LEE (Hongik University)

Checker Design for On-line Testing of Xilinx FPGA Communication

Zdenek KOTASEK, Martin STRAKA, Jiri TOBOLA (Brno University of Technology)

Defect-Tolerant Gate Macro Mapping & Placement in Clock-Free Nanowire Crossbar Architecture

Ravi BONAM (Univ. of Missouri-Rolla), Yong-Bin KIM (Northeastern Univ.), Minsu CHOI (Univ. of Missouri-Rolla)

Delay fault detection problems in circuits featuring a low combinational depth

Michele FAVALLI (Univ. of Ferrara)

Empirical Analysis of the Dependence of Test Power, Delay, Energy and Fault Coverage on the Architecture of LFSR-Based TPGs

Mehdi KAMAL (SRRF), Somayyeh KOOHI, Shaahin HESSABI (Sharif University of Technology)

Fault Tolerant Arithmetic Operations with Multiple Error Detection and Correction

Mojtaba VALINATAJ, Saeed SAFARI (Univ. of Tehran)

Probabilistic Analysis of Defect-Tolerant Gate Design Mapping in Asynchronous Nanowire Crossbar Architecture

Shikha CHAUDHARY, Minsu CHOI (Univ. of Missouri-Rolla)

Test Generation for Single and Multiple Stuck-at Faults of a Combinational Circuit Designed by Covering Shared ROBDD with CLBs

Anjela MATROSOVA, Ekaterina LOUKOVNIKOVA, Sergei OSTANIN, Alexandra ZINCHUCK, Ekaterina NIKOLAEVA (Tomsk State University)

Testing of Asynchronous NULL Conventional Logic (NCL) Circuits in Synchronous-Based Designs

Waleed K. AL-ASSADI, Sindhu KAKARLA (Univ. of Missouri-Rolla)

Production Yield and Self-Configuration in the future Massively Defective Nanochips

Piotr Zajac, Jacques Henri Collet (CNRS)

Timing-Aware Diagnosis for Small Delay Defects

Takashi AIKYO (Semiconductor Technology Academic Research Center), Hiroshi TAKAHASHI, Yoshinobu HIGAMI, Junichi OOTSU, Kyohei ONO, Yuzo TAKAMATSU (Ehime University)

Welcome cocktail

SEPTEMBER 27

8:30 – 9:50 Session 5 – Testing and Design for Testability

Session Chair: Renato Stefanelli
(Politecnico di Milano)

A-Diagnosis: A Complement to Z-Diagnosis Irith POMERANZ (Purdue University), Sudhakar REDDY (University of Iowa)

Test Generation and Diagnostic Test Generation for Open Faults with Considering Adjacent Lines Hiroshi TAKAHASHI, Yoshinobu HIGAMI, Yuzo TAKAMATSU (Ehime University)

Analysis of Specified Bit Handling Capability of Combinational Expander Networks Abhijit JAS, Srinivas PATIL (Intel Corporation)

Reduction of Fault Latency in Sequential Circuits by using Decomposition

Ilya LEVIN, Benjamin ABRAMOV, Vladimir OSTROVSKY (Tel Aviv University)

9:50 – 10:10 Coffe break

10:10 – 11:10 Session 6 – Soft Errors

Session Chair: Regis Leveugle
(TIMA Laboratory)

Soft Error Hardening for Asynchronous Circuits Weidong KUANG, Casto Manuel IBARRA (University of Texas – Pan American), Peiyi ZHAO (Chapman University)

Soft Error Hardened Latch Scheme for Enhanced Scan Based Delay Fault Testing

Takashi IKEDA, Kazuteru NAMBA, Hideo ITO (Chiba University)

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An Effective Approach for the Diagnosis of Transition-Delay Faults in SoCs, based on SBST and Scan Chains

Edgar E. SANCHEZ SANCHEZ (Politecnico di Torino), Davide APPELLO (STMicroelectronics), Matteo SONZA REORDA, Paolo BERNARDI, Michelangelo GROSSO (Politecnico di Torino), Jorge Luis LAGOS-BENITES (Pontificia Universidad Católica del Perú), Danilo RAVOTTO (Politecnico di Torino)

11:10 – 11:30 Short break

11:30 – 12:30 Session 7 – Defect and Fault Tolerance (2)

Session Chair: Dimitris Gizopoulos (University of Piraeus)

Improving the Tolerance of Pipeline Based Circuits to Power Supply or Temperature Variations

Jorge SEMIAO (Escola Superior de Tecnologia – Universidade do Algarve), Juan J. RODRIGUEZ-ANDINA (University of Vigo), Fabian VARGAS (Catholic University – PUCRS), Marcelino BICHO DOS SANTOS (IST/INESC-ID), Isabel TEIXEIRA (INESC-ID), Joao Paulo TEIXEIRA (IST, Lisboa Technical University)

RAM-based Fault Tolerant state machines for FPGAs

Laura FRIGERIO, Fabio SALICE (Politecnico di Milano)

Spare Parts in Analog Circuits: a Filter Example

Erik SCHULER, Adão DE SOUZA JUNIOR, Luigi CARRO (Universidade Federal Rio Grande do Sul)

12:30 – 13:40 Lunch

13:40 – 14:40 Session 8 – Dependable solutions for Memories and Storage

Session Chair: Israel Koren (University of Massachusetts)

A Sharable Built-in Self-repair for Semiconductor Memories with 2-D Redundancy Scheme

Swapnil BAHL (STMicroelectronics)

Matrix Codes: Multiple Bit Upsets Tolerant Method for SRAM Memories

Costas ARGYRIDES, Hamid R. ZARANDI, Dhiraj K. PRADHAN (Bristol University)

Reconstruction of Erasure Correcting Codes for Dependable Distributed Storage System without Spare Disks

Haruhiko KANEKO, Eiji FUJIWARA (Tokyo Institute of Technology)

14:40 – 14:50 Short break

14:50 – 15:50 Session 9 – Reliable Design Techniques (2)

Session Chair: Fabrizio Lombardi (Northeastern University)

Lazy Error Detection for Microprocessor Functional Units

Mahmut YILMAZ, Albert MEIXNER, Sule OZEV, Daniel SORIN (Duke University)

Effective Checkpoint and Rollback Using Hardware/OS Collaboration

Michele PORTOLAN (TIMA Laboratory), Regis LEVEUGLE (TIMA Laboratory)

On-Line Periodic Self-Testing of High-Speed Floating-Point Units in Microprocessors

George XENOULIS, Mihalis PSARAKIS, Dimitris GIZOPOULOS (University of Piraeus), Antonis PASCHALIS (University of Athens)

15:50 – 16:10 Coffee break

16:10 – 18:30 Panel

On-Chip Reliability Availability Serviceability (RAS) Design Costs: Can processors in consumer systems encroach in the high end space today?

Moderator: Prashant Joshi (Intel)

Banquet

SEPTEMBER 28

8:30 – 9:30 Keynote Address

Bringing Mainframe-Class Reliability to Mainstream Computing: Opportunities and Challenges

Rajesh Galivance (Intel)

9:30 – 11:10 Session 10 – Emerging technologies (1)

Session Chair: Marco Ottavi (Advanced Micro Devices)

A Scalable Framework for Defect Isolation of DNA Self-assembled Networks

Masaru FUKUSHI, Susumu HORIGUCHI (Tohoku University), Luke DEMORACSKI, Fabrizio LOMBARDI (Northeastern University)

Error Tolerance of DNA Self-Healing Assemblies by Puncturing

Masoud HASHEMPOUR, Zahra MASHREGHIAN ARANI, Fabrizio LOMBARDI (Northeastern University)

Fault Secure Encoding and Decoding for Nanotechnology Memory Architecture

Helia NAEIMI (Caltech), Andre DEHON (University of Pennsylvania)

Safety Evaluation of NanoFabrics

Michelangelo GROSSO, Maurizio REBAUDENGO, Matteo SONZA REORDA (Politecnico Di Torino)

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Nanofabric PLA architecture with Redundancy Enhancement

Waleed AL-ASSADI, Mandar JOSHI (University of Missouri-Rolla)

11:20 – 11:40 Coffee break

11:40 – 12:40 Session 11 – Testing

Session Chair: Luigi Carro
(Univ. Federal Rio Grande do Sul)

Hierarchical Fault Compatibility Identification for Test Generation with a Small Number of Specified Bits

Stelios N. NEOPHYTOU, Maria MICHAEL (University of Cyprus)

High quality test vectors for bridging faults in the presence of IC's parameters variations

Michele FAVALLI (University of Ferrara), Marcello DALPASSO (University of Padova)

Semi-Concurrent On-Line Testing of Transition Faults Through Output Response Comparison of Identical Circuits

Irith POMERANZ (Purdue University), Sudhakar REDDY (University of Iowa)

12:40 – 13:50 Lunch

13:50 – 14:50 Session 12 – Emerging technologies (2)

Session Chair: Maurizio Rebaudengo
(Politecnico di Torino)

Testing Reversible One-Dimensional QCA Arrays for Multiple Faults

Jing HUANG, Xiaojun MA (Northeastern University), Cecilia METRA (University of Bologna), Fabrizio LOMBARDI (Northeastern University)

Probabilistic Analysis of a Molecular Quantum-Dot Cellular Automata Adder

Timothy J DYSART, Peter KOGGE (University of Notre Dame)

On the Error Effects of Random Clock Shifts in Quantum-dot Cellular Automata Circuits

Marco OTTAVI (AMD), Faizal KARIM (University of British Columbia), Hamid HASHEMPOUR (LTX), Vamsi VANKAMAMIDI (Northeastern University), Konrad WALUS (University of British Columbia)

14:50 – 15:00 Short break

15:00 – 16:20 Session 13 – Reliable Applications

Session Chair: Cecilia Metra
(Università di Bologna)

Evaluation of Register-Level Protection Techniques for the Advanced Encryption Standard by Multi-Level Fault Injections

Paolo MAISTRI (TIMA Laboratory), Regis LEVEUGLE (TIMA Laboratory), Pierre VANHAUWAERT (TIMA Laboratory)

Power Attacks Resistance of Cryptographic S-boxes in presence of Error Detection Procedures

Francesco REGAZZONI (ALaRI - University of Lugano), Thomas EISENBARTH (Ruhr Universitaet Bochum), Johann GROSZSCHAEDL (University of Bristol), Luca BREVEGLIERI (Politecnico di Milano), Paolo IENNE (EPFL), Israel KOREN (University of Massachusetts), Christof PAAR (Horst Goertz Institute)

A Fault-Tolerant Active Pixel Sensor to Correct In-Field Hot Pixel Defects

Jozsef DUDAS, Michelle LA HAYE, Jenny LEUNG, Glenn CHAPMAN (Simon Fraser University)

Quantitative Analysis of In-Field Defects in Image Sensor Arrays

Jenny LEUNG, Jozsef DUDAS, Glenn CHAPMAN (Simon Fraser University), Israel KOREN, Zahava KOREN (University of Massachusetts)

16:20 – 16:30 Closing remarks

Co-Sponsored by:

- IEEE Computer Society
- IEEE Fault-Tolerant Computing Technical Committee
- IEEE Test Technology Technical Council



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