



33rd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

(DFT 2020)

Technical Program

October 19-21, 2020

- ❖ The time is in CEST zone
- ❖ (L) stands for Long papers and (S) stands for Short papers
- ❖ The duration of the presentation for Long papers is 20 minutes (15 min speech and 5 min Q&A) and for Short papers is 10 minutes (8 min speech and 2 min Q&A)

DAY 1 – Monday October 19, 2020

13.00-13.30: Opening Session

General chairs: Gianluca Furano, Marco Ottavi

Program chairs: Luigi Dilillo, Mihalis Psarakis

13.30-14.20: Session #1 – Testing Methods-1

Chair : Ernesto Sanchez

- ❖ (L) A Multiple Target Test Generation Method for Gate-Exhaustive Faults to Reduce the Number of Test Patterns Using Partial MaxSAT
Ryuki Asami, Toshinori Hosokawa, Masayoshi Yoshimura and Masayuki Arai
- ❖ (L) Power-aware Test Scheduling for IEEE 1687 Networks with Multiple Power Domains
Payam Habiby, Sebastian Huhn and Rolf Drechsler
- ❖ (S) Reducing DFT hardware overhead by use of a test microprogram in a microprogrammed hardware accelerator
Maryam Rajabalipanah, Seyedeh Maryam Ghasemi, Nooshin Nosrati, Katayoon Basharkhah, Saba Yousefzadeh and Zainalabedin Navabi

10 min break

14.30 -15.30: Keynote #1 - Living with imprecise computation: an energy efficiency perspective

by Prof. Luca Benini, Universita di Bologna

Chair: Marco Ottavi

10 min break

15.40-16.30: Session #2 - Fault Tolerance Techniques

Chair : Paolo Rech

- ❖ (L) Lightweight Fault Detection and Management for Image Restoration
Cristiana Bolchini, Luca Cassano, Antonio Miele and Matteo Biasielli

- ❖ (L) Radiation Hardening Legalisation Satisfying TMR Spacing Constraints with Respect to HPWL
Christos Georgakidis and Christos Sotiriou
- ❖ (S) 2D Error Correction for F/F based Arrays using In-Situ Real-Time Error Detection (RTD)
Yiannakis Sazeides, Arkady Bramnik, Ron Gabor, Chrysostomos Nicopoulos, Ramon Canal, Dimitris Konstantinou and Giorgos Dimitrakopoulos

16.30-17.30: Session #3 - Dependability of Real-Time Systems and Network-on-Chip

Chair: Ramon Canal

- ❖ (L) Markov Chain-based Modeling and Analysis of Checkpointing with Rollback Recovery for Efficient Design Space Exploration in Soft Real-time Systems
Siva Satyendra Sahoo, Bharadwaj Veeravalli and Akash Kumar
- ❖ (L) On the Analysis of Real-time Operating System Reliability in Embedded Systems
Dario Mamone, Alberto Bosio, Alessandro Savino, Maurizio Rebaudengo and Said Hamdioui
- ❖ (L) A novel Network-on-Chip security algorithm for tolerating Byzantine faults
Soultana Ellinidou, Gaurav Sharma, Olivier Markowitch, Jean-Michel Dricot and Guy Gogniat

10 min break

17.40-18.40: Session #4 - Technology and Reliability-aware Design Issues

Chair: Prashant D. Joshi

- ❖ (L) Sensing with Memristive Complementary Resistive Switch: Modelling and Simulations
Vishal Gupta, Danilo Pellegrini, Saurabh Khandelwal, Abusaleh Jabir, Shahar Kvatinsky, Eugenio Martinelli, Corrado Di Natale and Marco Ottavi
- ❖ (L) Efficient LDPC Encoder Designs for Magnetic Recording Media
Dimitris Theodoropoulos, Nektarios Kranitis, Antonis Tsigkanos and Antonis Paschalis
- ❖ (S) Resistive RAM SET and RESET Switching Voltage Evaluation as an Entropy Source for Random Number Generation
Hussein Bazzi, Jeremy Postel-Pellerin, Hassen Aziza, Mathieu Moreau and Adnan Harb
- ❖ (S) Using digital imagers to characterize the dependence of energy and area distributions of SEUs on elevation
Glenn Chapman, Rohan Thomas, Klinsmann Joel J. Coelho Silva Meneses, Israel Koren and Zahava Koren

DAY 2 – Tuesday October 20, 2020

13.00–13.40: Session #5 - Neural Networks Dependability-1

Chair: Alberto Bosio

- ❖ (L) Evaluation of Pruned Neural Networks against Errors on Parameters
Zhen Gao, Xiaohui Wei, Han Zhang, Wenshuo Li, Guangjun Ge, Yu Wang and Pedro Reviriego Reliability
- ❖ (S) Reliable Classification with Ensemble Convolutional Neural Networks
Zhen Gao, Han Zhang, Xiaohui Wei, Wenshuo Li, Yu Wang and Pedro Reviriego

- ❖ (S) Evaluating Data Encryption Effects on the Resilience of an Artificial Neural Network
Nikolaos Deligiannis, Marcello Traiola, Emanuele Valea, Matteo Sonza Reorda and Riccardo Cantoro

13.40-14.40: Keynote #2 - Fault-Tolerance in Current and Future LEON and NOEL-V System-on-Chip Architectures

by Jan Andersson, Cobham Gaisler

Chair: Gianluca Furano

10 min break

14.50-15.50: Session #6 - Neural Networks Dependability-2

Chair: Pedro Reviriego

- ❖ (L) Investigating the Impact of Radiation-Induced Soft Errors on the Reliability of Approximate Computing Systems
Lucas Matana Luza, Daniel Söderström, Georgios Tsiligiannis, Helmut Puchner, Carlo Cazzaniga, Ernesto Sanchez, Alberto Bosio and Luigi Dilillo
- ❖ (L) A Pipelined Multi-Level Fault Injector for Deep Neural Networks
Annachiara Ruospo, Angelo Balaara, Alberto Bosio and Ernesto Sanchez
- ❖ (S) An Emulation Platform for Evaluating the Reliability of Deep Neural Networks
Corrado De Sio, Sarah Azimi and Luca Sterpone
- ❖ (S) Impact of Layers Selective Approximation on CNNs Reliability and Performance
Rubens Luiz Rech Junior and Paolo Rech

15.50-16.40: Session #7 - AI in space

Chair: Marco Rovatti

- ❖ (L) On board satellite telemetry forecasting with RNN on RISC-V based multi core processor
Danilo Cappellone, Gianluca Furano, Stefano Di Mascio, Alessandra Menicucci and Marco Ottavi
- ❖ (L) Hardware Accelerator Design with Supervised Machine Learning for Solar Particle Event Prediction
Junchao Chen, Thomas Lange, Marko Andjelkovic, Aleksandar Simevski and Milos Krstic
- ❖ (S) AI in space: applications examples and challenges
Gianluca Furano, Marco Rovatti and Antonis Tavoularis

10 min break

16.50-17.50: Session #8 - Testing Methods-2

Chair : Hassen Aziza

- ❖ (L) EVM measurement of RF ZigBee transceivers using standard digital ATE
Thibault Vayssade, Florence Azais, Laurent Latorre and Francois Lefevre
- ❖ (L) Variation-Aware Test for Logic Interconnects using Neural Networks – A Case Study
Alexander Sprenger, Somayeh Sadeghi-Kohan, Jan Dennis Reimer and Sybille Hellebrand

- ❖ (S) Observability Driven Path Generation for Delay Test Coverage Improvement in Scan Limited Circuits
Avijit Chakraborty and Duncan Walker
- ❖ (S) Improving a Test Set to Cover Test Holes by Detecting Gate-Exhaustive Faults
Irith Pomeranz

DAY 3 – Wednesday October 21, 2020

13.00-14.00: Special Session #1 - Latest Trends in Hardware Security and Privacy

Chair: Giorgio Di Natale

Giorgio Di Natale, Francesco Regazzoni, Vincent Albanese, Frank Lhermet, Yann Loisel, Abderrahmane Sensaoui and Samuel Pagliarini

- ❖ (L) WorldGuard, a SoC-level isolation solution
Yann Loisel
- ❖ (L) Reimagining Software Threats And Defences In Hardware
Samuel Pagliarini

14.00 -15.00: Keynote #3 - Design Rationales for Fail-Operational Safety Platforms

by Dr. Wilfried Steiner, TTTech Labs

Chair: Luigi Dilillo

10 min break

15.10-16.10: Session #9 - Hardware Security

Chair: Samuel Pagliarini

- ❖ (L) Clock Glitch versus SIFA
Aein Rezaei Shahmirzadi and Amir Moradi
- ❖ (L) You can detect but you cannot hide: Fault Assisted Side Channel Analysis on Protected Software-based Block Ciphers
Athanasios Papadimitriou, Konstantinos Nomikos, Mihalis Psarakis, Ehsan Aerabi and David Hely
- ❖ (S) A Modelling Attack Resistant Low Overhead Memristive Physical Unclonable Function
Xiaohan Yang, Saurabh Khandelwal, Aiqi Jiang and Abusaleh Jabir
- ❖ (S) A Lightweight Reconfigurable RRAM-based PUF for Highly Secure Applications
Basma Hajri, Hassen Aziza, Mohammad Mansour and Ali Chehab

16.10-17.10: Session #10 - Microprocessors Reliability and Validation

Chair: Luca Cassano

- ❖ (L) Fault resilience analysis of a RISC-V microprocessor design through a dedicated UVM environment
Marcello Barbirotta, Antonio Mastrandrea, Francesco Menichelli, Francesco Vigli, Luigi Blasi, Abdallah Cheikh, Fabio Di Gennaro, Stefano Sordillo and Mauro Olivieri

- ❖ (L) Validation Challenges in Recent Trends in Power Management in Microprocessors
Nagabhushan Reddy, Sankaran Menon and Prashant Joshi
- ❖ (S) Software-only based Diverse Redundancy for ASIL-D Automotive Applications on Embedded HPC Platforms
Sergi Alcaide Portet, Leonidas Kosmidis, Carles Hernandez and Jaume Abella

17.10-17.30: Concluding Session