

## JETTA – Special Issue on Defect and Fault Tolerance

Guest Editors: Prashant D. Joshi, Massimo Violante

Semiconductor technologies are offering impressive breakthrough each time a new generation hits the market. Along with higher transistor density, higher operation frequency, and lower power consumption, ultra-deep submicron technologies also bring new concerns to developers. Precise control of the manufacturing process is needed to achieve economically sustainable yield; advanced test techniques based on newer fault models than traditional stuck-at are mandatory to meet the quality levels that customers expect; fault tolerance and self repair capabilities are required to survive the misbehavior induced by the environment (like for example transient errors originated by the interaction of silicon with radioactive particles), and to overcome failures that may occur during the operational lifetime of the system.

Developers, being them from traditional fault tolerant domains such as automotive, railway, avionic, as well as developers of commodity applications that must guarantee the highest quality for their mass-market products, face the mentioned issues, and must rely on suitable defect and fault tolerance techniques.

The purpose of this special issue is to provide an overview of the most up-to-date topics in defect and fault tolerance in ultra-deep submicron technologies, including but not limited to:

- **Yield Analysis and Modeling:** Defect/Fault analysis and models; statistical yield modeling; critical area and other metrics.
- **Testing Techniques:** Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; signal and clock integrity.
- **Error Detection, Correction, and Recovery:** Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques.
- **Design For Testability in IC Design:** FPGA, SoC, NoC, ASIC, microprocessors.
- **Dependability Analysis and Validation:** Fault injection techniques and environments; dependability characterization.
- **Defect and Fault Tolerance:** Reliable circuit & system synthesis; radiation hardened/tolerant processes & design; design space exploration for dependable systems, transient/soft faults and errors.
- **Repair, Restructuring and Reconfiguration:** Repairable logic, reconfiguration, repair; reconfigurable circuit design; DFT for on-line operation; self-healing.
- **Totally Fail-Safe Design for Critical Applications:** Methodologies and case study applications to automotive, railway, avionics, industrial control, biomedicine, space and smart power networks.

Authors should submit previously unpublished papers to the manuscript submission website <http://www.editorialmanager.com/jetta/> specifying the article type as "D&FT11". Expanded versions of conference papers are also welcome. Please follow the author instructions available at <http://www.springer.com/10836> when submitting your paper. The final selections will be made through the journal's peer review process. The schedule is as follows:

Paper submission deadline:	February 24 <sup>th</sup> , 2012
Acceptance/revision/rejection notification:	May 18 <sup>th</sup> , 2012
Final manuscript:	June 15 <sup>th</sup> , 2012
Tentative publication date:	December 2012

### Guest Editors

Prashant D. Joshi  
Intel  
DEG DAP-Special Operations  
1501 S. Mopac, Suite 400  
Austin, Tx 78746  
USA  
prashant.d.joshu@intel.com

Massimo Violante  
Politecnico di Torino  
Dip. Automatica e Informatica  
C.so Duca degli Abruzzi 24  
10129 Torino  
ITALY  
massimo.violante@polito.it