IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

30th edition!

October 23–25, 2017 @ Cambridge, UK

Call for Papers

DFT is an annual Symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following:

1. Yield Analysis and Modeling: Defect/fault analysis and models; statistical yield modeling; diagnosis; critical area and other metrics.

2. Testing Techniques: Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; online testing; signal and clock integrity.

3. Design for Testability in IC Design: FPGA, SoC, NoC, ASIC, low power design and microprocessors.

4. Error Detection, Correction, and Recovery: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques; architectural-specific techniques, system-level design-time or runtime strategies.

5. Dependability Analysis and Validation: Fault injection techniques and frameworks; dependability and characterization.

6. Repair, Restructuring and Reconfiguration: Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing; reliable FPGA-based systems.

7. Defect and Fault Tolerance: Reliable circuit/system synthesis; radiation hardened and/or tolerant processes and design; design space exploration for dependable systems, transient/soft faults and errors.

8. Aging and Lifetime Reliability: Aging characterization and modeling; design and run-time reliability, thermal, and variability management and recovery.

9. Dependable Applications and Case Studies: Methodologies and case study applications to Internet of Things, automotive, railway, avionics and space, autonomous systems, industrial control, etc.

10. Emerging Technologies: Techniques for 2.5D/3D ICs, quantum computing architectures, microfluid biochips, etc.

11. Design for Security: Fault attacks, fault tolerance-based countermeasures, hw security assurance, hw trojans, resistance to persistent DoS, security vs. reliability trade-offs, interaction between VLSI test, trust, and reliability.

Paper Submission: Prospective authors are invited to submit original and unpublished contributions. Two types of submissions are possible: (i) regular papers (6 pages), and (ii) short papers (4 pages). Both types will be included in the symposium proceedings and should adhere to the IEEE conference template, 2-columns style (available on conference web site), and submitted as a PDF file, electronically. Please refer to the symposium web page for updated information.

Call for Special Sessions: Proposals for Special Sessions are also invited. For more information, visit symposium website and see the specific call.

Paper Publication: Only original, unpublished work will be accepted, for regular or short presentation at the symposium. Proceedings will be published by the *IEEE Computer Society* and will appear in the *Digital Library*. Furthermore, selected papers will be considered for a special issue in the IET Computers & Digital Techniques.

Awards: All papers will be considered for the DFT 2017 Best Paper Award. A best Student Paper Award (funded by Cadence) will be assigned to the best paper having a student as first author.

Author Registration: Every accepted paper MUST have at least one *full* paid registration by the time the camera-ready paper is submitted for inclusion in the proceedings, and one of the authors is expected to attend the Symposium and present the paper.

Venue: The symposium is returning to Europe on its 30th anniversary and will take place in UK at the Moller Centre (Churchill College), situated in the beautiful university city of Cambridge. The city is conveniently located close to London, and connected by excellent rail services and international flights through multiple airports.

Prospective authors should adhere to the following deadlines:

Paper submission:	**April 28, 2017**
Notification of acceptance:	**July 1, 2017**
Camera ready and author's registration:	**July 21, 2017**

Sponsored by: IEEE computer society, TCFT, tttc, IEEE

DFT 2017 webpage: http://www.dfts.org Twitter: @DFTSymposium