IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

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Call for Papers

DFT is an annual Symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following:

1. Yield Analysis and Modeling: Defect/Fault analysis and models; statistical yield modeling; critical area and metrics.
2. Testing Techniques: Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; signal and clock integrity.
3. Design For Testability in IC Design: FPGA, SoC, NoC, ASIC, microprocessors.
4. Error Detection, Correction, and Recovery: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques.
5. Dependability Analysis and Validation: Fault injection techniques and environments; dependability characterization.
6. Repair, Restructuring and Reconfiguration: Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing.
7. Defect and Fault Tolerance: Reliable circuit/system synthesis; radiation hardened and/or tolerant processes & design; design space exploration for dependable systems, transient/soft faults and errors.
8. Totally Fail-Safe Design for Critical Applications: Methodologies and case study applications to automotive, railway, avionics, industrial control, biomedicine, space and smart power networks.
9. Emerging Technologies: Techniques for CNTs, QCA, DNA, RTDs, SETs, molecular devices and self-assembly.
10. Hardware security: Fault attacks, fault tolerance-based counter-measures, Scan-based attacks and counter-measures, hardware trojans, security vs reliability trade-offs, interaction between VLSI test, trust, and reliability.

Paper Submission: Prospective authors are invited to submit original and unpublished contributions. Two types of submissions are possible: (i) regular papers (6 pages - with the opportunity to purchase 2 additional ones), and (ii) short papers (4 pages) to be presented as posters. Both types will be included in the symposium proceedings and should adhere to the IEEE conference template, 2-columns style (available on conference web site), and submitted as PDF file, electronically. Please refer to the symposium web page for updated information.
We are also interested in panel sessions that involve industrial experiences: please send an email to the Program co-Chairs with a brief description (1 page max) of the proposed panel.

Paper Publication: Only original, unpublished work will be accepted, for regular or poster presentation at the symposium. Proceedings will be published by the *IEEE Computer Society* and will appear in the *Digital Library*. Furthermore, selected papers will be considered for a special issue/section of *IEEE Transactions on Emerging Topics in Computing* (confirmed).

Best Paper Award: All papers will be considered for the *DFTS 2015 Best Paper Award*.

Author Registration: Every accepted paper MUST have at least one *full* paid registration by the time the camera-ready paper is submitted for inclusion in the proceedings, and the author is expected to attend the Symposium and present the paper.

Prospective authors should adhere to the following deadlines:

Abstract Submission deadline:	**May 8th, 2015**
Paper Submission deadline (extended):	**May 18th, 2015**
Notification of acceptance (extended):	**July 13th, 2015**
Camera ready full papers:	**August 7th, 2015**

For general information, contact the General co-Chairs. For paper submission information, contact the Program co-Chairs. For all updated information, visit our web page.

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