# Technical Program of the 28th DFT Symposium

## Monday, October 12th, 2015

**09:00-10:00** Registration

**10:00-10:15** Conference Opening

S. Kundu and S. Pontarelli, General Chairs
O. Khan and M. K. Michael, Program Chairs

**10:15-11:15** Keynote Talk 1

Reliable System Design in the Era of Specialization
*David Brooks, Harvard University*

**11:15-11:25** Short Break

**11:25-12:25** Session 1: Memories and Emerging Technologies

Session Chair: TBA

1.1R Evaluating the Impact of Spike and Flicker Noise in Phase Change Memories
*S. Junsangsri, F. Lombardi, and J. Han*

1.2R A Fault Detection and Repair of DSC Arrays through Memristor Sensing
*J. Mathew, Y. Yang, M. Ottavi, T. Brown, A. Zampetti, A. Di Carlo, A. M. Jabir and D. K. Pradhan*

1.3R Asymmetric ECC Organization in 3D-Memory via Spare Column Utilization
*H. Han and J.-S. Yang*

1.4S Exploring Error-Tolerant Low-Power Multiple-output Read Scheme for Memristor-Based Memory Arrays
*A. Adeyemo, J. Mathew, A. Jabir and D. K. Pradhan*

**12:30-13:50** Lunch Break

**13:50-15:30** Session 2: Best Paper Candidates

Session Chair: TBA

2.1R RotR: Rotational Redundant Task Mapping for Fail-operational MPSoCs
*B. Nahar and B. H. Meyer*

2.2R On Enhancing the Debug Architecture of a System-on-Chip (SoC) to Detect Software Attacks
*J. Backer, D. Hely and R. Karri*

2.3R Software-Based On-Chip Thermal Sensor Calibration for DVFS-enabled Many-core Systems
*S. Terävänen, M.-H. Haghbayan, A.-M. Rahmani, P. Liljeberg and H. Tenhunen*

2.4R Single Event Upsets and Hot Pixels in Digital Imagers
*G. H. Chapman, R. Thomas, R. Thomas, K. J. Meneses, T. Yang, I. Koren and Z. Koren*

2.5R Accelerated Microarchitectural Fault Injection-Based Reliability Assessment
*M. Kaliorakis, S. Tselonis, A. Chatzidimitriou and D. Gizopoulos*

**15:30-16:00** Coffee Break

**16:00-16:20** Invited Talk

Achievements of the COST Action MEDIAN
*Marco Ottavi, University of Rome "Tor Vergata"*

**16:20-17:40** Session 3: Fault Tolerance

Session Chair: TBA

3.1R Hot Spare Components for Performance-Cost Improvement in Multi-core SIMT
*S. H. Mozafari and B. H. Meyer*

3.2R Low-Overhead Fault-Tolerance for the Preconditioned Conjugate Gradient Solver
*A. Schoell, C. Braun, M. A. Kochte and H.-J. Wunderlich*

3.3R *On-line Detection of Intermittent Faults in Digital-to-Analog Converters*
*M. Soma*

3.4S A Dual-Layer Fault Manager for Systems based on Xilinx Virtex FPGAs
*I. Herrera-Alzu, M. Lopez Vallejo and C. Gil-Soriano*

3.5S REPAIR: Hard-Error Recovery via Re-Execution
*J. Soman, N. Miralaei, A. Mycroft, T. Jones*

## Tuesday, October 13th, 2015

**08:00-08:30** Registration

**08:30-09:30** Keynote Talk 2

Statistical Correlation Driven Testing, Process Diagnosis and Tuning:
The Signature Testing Paradigm and Beyond
*Abhijit Chatterjee, Georgia Institute of Technology*

**09:30-10:30** Session 4: Soft Errors

Session Chair: TBA

4.1R A Method to Protect Bloom Filters from Soft Errors
*P. Revriiego, S. Pontarelli, J. A. Maestro and M. Ottavi*

4.2R Influence of triple-well technology on laser fault injection and laser sensor efficiency
*N. Borrel, C. Champeix, E. Kussener, W. Rahajandraibe, M. Lisart, A. Sarafianos and J.-M. Dutertre*

4.3R Using Value Similarity of Registers for Soft Error Mitigation
*A. Eker and O. Ergin*

**10:30-11:00** Coffee Break

**11:00-12:30** Session 5: Security

Session Chair: TBA

5.1R Security Analysis of Logic Encryption Against the Most Effective Side-Channel Attack: DPA
*M. Yasin, B. Mazumdar, Sk S. Ali and O. Sinanoglu*

5.2R Reliable Hash Trees for Post-quantum Stateless Cryptographic Hash-based Signatures
*M. Mozaffar-Kermani and R. Azarderakhsh*

5.3R Chip-level Anti-reverse Engineering using Transformable Interconnects
*S. Chen, J. Chen, D. Forte, J. Di, M. Tehranipoor and L. Wang*

5.4S Scan Attack on Elliptic Curve Cryptosystem
*Sk S. Ali and O. Sinanoglu*

5.5S Enhancing Embedded SRAM Security and Error Tolerance with Hardware CRC and Obfuscation
*S. Kan, M. Ottavi and J. Dworak*

5.6S A BIST Approach for Counterfeit Circuit Detection based on NBTI Degradation
*P. Savanur, P. Alladi and S. Tragoudas*

**12:30-13:40** Lunch Break

**13:40-15:00** Session 6: Test Generation and Fault Simulation

Session Chair: TBA

6.1R Quest for a Quantum Search Algorithm for Testing Stuck-at Faults in Digital Circuits
*M. Venkatasubramanian and V. D. Agrawal*

6.2R Piecewise-Functional Broadside Tests Based on Intersections of Reachable States
*I. Pomeranz*

6.3R Predictive LBIST Model and Partial ATPG for

Seed Extraction
*G. Contreras, N. Ahmed, L. Winemberg, and M. Tehranipoor*

6.4S A CMOS ripple detector for integrated voltage regulator testing
*C. Ozmen, A. Dirican, N. Tan, H. Nguyen and M. Margala*

6.5S Adaptive Fault Simulation on Many-core Microprocessor Systems
*M.-H. Haghbayan, S. Terävänen, A.-M. Rahmani, P. Liljeberg and H. Tenhunen*

**15:00-15:10** **Short Break**

**15:10-16:00** **Session 7: Test Compaction and Compression**

Session Chair: TBA

7.1R Compacting Output Responses Containing Unknowns Using an Embedded Processor
*K. Saleem, S. Muthyala and N. Touba*

7.2R Impact of Test Compression on Power Supply Noise Control
*T. Zhang and D. M. H. Walker*

7.3S Improving X-Tolerant Combinational Output Compaction via Input Rotation
*A. Bawa and N. Touba*

**16:00-16:30** **Coffee Break**

**16:30-17:30** **Session 8: Resilient Design and Technology**

Session Chair: TBA

8.1R Low-Power LDPC Decoder Design Exploiting Memory Error Statistics
*J. Chen and L. Wang*

8.2R SEU sensitivity and modeling using picosecond pulsed laser stimulation of a D Flip-Flop in 40 nm CMOS technology
*C. Champeix, N. Borrel, J.-M. Dutertre, B. Robisson, M. Lisart and A. Sarafianos*

8.3S Approximate Compressors for Error-Resilient Multiplier Design
*Z. Yang, J. Han and F. Lombardi*

8.4S Characterization of low power radiation-hard Reed-Solomon code protected serializers in 65-nm for HEP experiments electronics
*D. Felici, S. Bonacini and M. Ottavi*

**17:30-18:30** **DFTS TPC Meeting**

## Wednesday, October 14th, 2015

**08:00-08:30** **Registration**

**08:30-09:30** **Keynote Talk 3**

Building a Resilient Internet of Things
*Rob Aitken, ARM*

**09:30-10:40** **Session 9: Resilience in Many-core Systems**

Session Chair: TBA

9.1R Reducing the Performance Overhead of Resilient CMPs with Substitutable Resources
*A. Malek, S. Tzilis, D. A. Khan, I. Sourdis, G. Smaragdos and C. Strydis*

9.2R Dependable Real-Time Task Execution Scheme for a Many-core Platform
*T. Yoneda, M. Imai, H. Saito and K. Kise*

9.3R Towards Reliability and Performance-Aware Wireless Network-on-Chip Design
*M. O. Agyeman, K. Tong and T. Mak*

9.4S A Fast and Scalable Fault Injection Framework to Evaluate Multi/Many-core Soft Error Reliability
*F. Rosa, F. Kastensmidt, R. Reis and L. Ost*

**10:40-11:10** **Coffee Break**

**11:10-12:20** **Session 10: Error Prediction, Detection and Diagnosis**

Session Chair: TBA

10.1R A Cross-layer Approach to Online Adaptive Reliability Prediction of Transient Faults
*B. Farahani and S. Safari*

10.2R A non-conservative software-based approach for detecting illegal CFE's caused by transient faults
*D. Rodrigues, G. Nazarian, Á. Moreira, L. Carro and G. Gaydadjiev*

10.3R A Configurable Board-level Adaptive Incremental Diagnosis Technique based on Decision Trees
*C. Bolchini and L. Cassano*

10.4S IntelliCAN: Attack-Resilient Controller Area Network (CAN) for Secure Automobiles
*M. R. Ansari, S. Yu and Q. Yu*

**12:20-12:30** **Conference Closing**

**12:30** **Boxed Lunch**

# Program of the 28th IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

## October 12-14, 2015

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