IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium

September 19-20, 2016

University of Connecticut
Storrs, CT USA

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Monday, Sept. 19

8:00-8:30 Registration & Continental Breakfast

8:30-8:45 Opening Remarks by DFT 2016 General and Program Chairs

8:45-9:45 KEYNOTE 1:
Session Chair: Antonio Miele (Politecnico di Milano)
Speaker: Vilas Sridharan, AMD Inc.
Title: Memory Errors in Modern Systems

Session 1: Aging
Session Chair: Fabrizio Lombardi (Northeastern U.)

9:45-10:25
(L)* BTI Aware Thermal Management for Reliable DVFS Designs
H. Chahal, V. Tenentes, D. Rossi, and B. Al-Hashimi (U. Southampton)
(S) Prognosis of NBTI Aging Using a Machine Learning Scheme
N. Karimi (Rutgers U.) and K. Huang (San Diego State U.)
(S) Experimental Study and Analysis of Soft and Permanent Errors in Digital Cameras
I. Koren[1], G. Chapman[2], R. Thomas[2], R. Thomas[2] and Z. Koren[1] ([1]Univ. of Massachusetts, [2]Simon Fraser University)

20 min Coffee Break

Session 2: Fault Tolerance in Latches & Approximate Computing
Session Chair: Naghmeh Karimi (Rutgers U.)

10:45-11:45
(L)* A Highly Robust Double Node Upset Tolerant Latch
A. Watkins (Los Alamos National Laboratories) and S. Tragoudas (Southern Illinois University Carbondale)
(L)* Applying Efficient Fault Tolerance to Enable the Preconditioned Conjugate Gradient Solver on Approximate Computing Hardware
A. Schoell, C. Braun and H.-J. Wunderlich (University of Stuttgart)
(S) Construction of A Soft Error (SEU) Hardened Latch with High Critical Charge
H. Ueno and K. Namba (Chiba Univ.)
(S) Design and Analysis of an Approximate 2D Convolver
F. Lombardi (Northeastern U.), J. Han (U. Alberta) and K. Chen (Northeastern U.)

* Best Paper Candidate

Lunch Break

Session 3: System-level Approaches
Session Chair: Akash Kumar (Technische Universitaet Dresden)

13:30-14:40
(L) Combined On-line Lifetime-Energy Optimization for Asymmetric Multicores
C. Bolchini (Politecnico di Milano), M. Carminati (Politecnico di Milano), T. Mitra (NUS, Singapore) and T. S. Muthukaruppan (NUS, Singapore)
(L) Effects of Online Fault Detection Mechanisms on Probabilistic Timing Analysis
C. Chen, J. Panerati and G. Beltrame (Ecole Polytechnique de Montreal)
(L) Bounding Error Detection Latency in Safety Critical Systems with Enhanced Execution Fingerprinting
M. Liu and B. Meyer (McGill U.)
(S) Guiding Genetic Algorithms Using Importance Measures for Reliable Design of Embedded Systems
H. Aliee[1], S. Vitzethum[1], M. Glaß[1], J.Teich[1] and [2]E.Borgonovo ([1]FAU, [2]Bocconi U.)

20 min Coffee Break

Session 4: Special Session on Fault-tolerant Realtime Systems
Session Chair: Giovanni Beltrame (Polytechnique Montreal)

15:00-16:10
(L) Fault-tolerant Scheduling of Multicore Mixed-Criticality Systems under Permanent Failures
Z. Al-Bayati[1], B. H. Meyer[1] and [2]H. Zeng ([1]McGiill U., [2]Virginia Tech)
(L) Cross-Layer Fault-Tolerant Design of Real-Time Systems
S. S. Sahoo (NUS, Singapore), B. Veeravalli (NUS, Singapore) and A. Kumar (Technische U. Dresden)
(L) Fault-Aware Sensitivity Analysis for Probabilistic Real-Time Systems
L. Santinelli (ONERA), Z. Guo (UNC) and L. George (LIGM – ESIEE)

Short Break

16:20-17:20 TPC Meeting

17:00-18:30 Reception

Tuesday, Sept. 20

8:00-8:30 Registration & Continental Breakfast

8:30-9:30
KEYNOTE 2:
Session Chair: Qiaoyan Yu (U. New Hampshire)
Speaker: Swarup Bhunia, University of Florida
Title: security versus test and reliability: the crossroads and beyond

Session 5: FPGA & CMOS Technologies
Session Chair: Swaroop Ghosh (PSU)

9:30-10:30
(L) Low Cost Resilient Regular Expression Matching on FPGAs
M. Leipnitz, E. N. de Souza and G. Nazar (U. Federal do Rio Grande do Sul)
(L) In-Place LUT Polarity Inversion to Mitigate Soft Errors for FPGAs
J. Su (UCLA), J.-Y. Lee (UCLA), C. Wu (Fudan U.) and L. He (UCLA, Fudan U.)
(S) Detecting Intermittent Resistive Faults in Digital CMOS Circuits
H. Ebrahimi, A. Rohani and H.G. Kerkhoff(U. Twente)
(S) Soft Error Vulnerability Assessment of the Real-Time Safety-Related ARM Cortex-R5 CPU
X. Iturbe, B. Venu and E. Ozer (ARM Research)

20 min Coffee Break

Session 6: Architecture-level Techniques
Session Chair: Brett Meyer (McGill U.)

10:50-11:40
(L) Efficient Utilization of Hierarchical iJTAG Networks for Interrupts Management
A. Ibrahim (U. Twente) and H. Kerkhoff (U. Twente / CTIT-TDT)
(S) Error Recovery Through Partial Value Similarity
A. Eker and O. Ergin (TOBB U. Economics and Technology)
(S) In-field functional test programs development flow for embedded FPUs
R. Cantoro[1], D. Piumatti[1], P. Bernardi[1], S. De Luca[2] and A. Sansonetti[2] ([1]Politecnico di Torino, [2]STMicroelectronics)
(S) Design and characterization of a high-safety hardware/software module for the acquisition of Eurobalise telegram
F. Giuliani[1], M. Ottavi[2], G. Cardarilli[2], M. Re[2], L. Di Nunzio[2], R. Fazzolari[2] A. Bruno[1] and F. Zuliani[1] ([1]NEAT S.r.l., [2]University of Rome "Tor Vergata")

Lunch Break

Award Announcement

13:30-14:30

Session 7: Fault tolerance in NoC & SoC
Session Chair: Qiaoyan Yu (U. New Hampshire)

(L) CoBRA: Low Cost Compensation of TSV failures in 3D-NoC
R. Salamat (UC Irvine), M. Ebrahimi(KTH), N. Bagherzadeh (UC Irvine) and F. Verbeek (Radboud U.)
(L) A New Approach to Deadlock-Free Fully Adaptive Routing for High-Performance Fault-Tolerant NoCs
A. Charif, N.-E. Zergainoh and M. Nicolaidis (TIMA Laboratory)
(S) An Adaptive Routing Algorithm to Improve Lifetime Reliability in NoCs Architecture
J. Alshraiedeh and A. Kodi (Ohio U.)
(S) A Novel Method for SEE validation of Complex SoCs Using Low-Energy Proton Beams
G. Furano[1], S. Di Mascio[1], T. Szewczyk[1], A.Menicucci[3], L. Campajola[4], F. Di Capua[4] A. Fabbri[5] and M. Ottavi[2] ([1]European Space Agency, [2]U. Rome "Tor Vergata", [3]TUDelft, [4]NaplesFederico II, [5]INFN, Roma Tre Section)

20 min Coffee Break

Session 8: Special Session on the use of VLSI Techniques for Securing ICs against Attacks
Session Chair: Sandip Kundu (UMass Amherst)

14:50-16:20
(L) Reliable PUF Design Using Failure Patterns from Time-Controlled Power Gating
X. Xu and D. Holcomb (U. Massachusetts, Amherst)
(L) Side Channel Attacks on STTRAM and Low-Overhead Countermeasures
A. Iyengar[1], S. Ghosh[1], N. Rathi[2] and H. Naeimi[3] ([1]Penn State U., [2]Purdue U., [3]Intel Corp.)
(L) On Meta-Obfuscation of Physical Layouts to Conceal Design Characteristics
V. C. Patil, A. Vijayakumar and S. Kundu (U. Massachusetts Amherst)
(L) Can Flexible, Domain Specific Programmable Logic Prevent IP Theft?
X. Cui[1], K. Wu[2], S. Garg[2] and R. Karri[2] ([1]Chongqing U., [2]NYU)

16:20-16:30 Closing Remarks

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