DFT 2018 The 31st IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

October 8—October 10, 2018, Chicago, IL, USA

Technical Program

Monday, October 8, 2018

08:00—09:00am Registration

09:00—10:00am Keynote #1: Redundancy and Testability Hit the Road for Resilient Autonomous Driving *N. R. Saxena* (NVIDIA)

10:00—10:30am Coffee Break

10:30—12:00pm Session 1—Memories *Chair: S. Tragoudas* (SIU)

- Complementary Resistive Switch Sensing (Best Paper Award Nominee) *D. Pellegrini, M. Ottavi, E. Martinelli, and C. di Natale* (Un. of Rome)
- Physics-Informed Machine Learning for DRAM Error Modeling *E. Baseman, N. DeBardeleben, S. Blanchard, J. Moore, O. Tkachenko, K. Ferreira, T. Siddiqua, and V. Sridharan* (LANL, NM Consortium, Sandia NL, Advanced Micro Devices)
- Construction of Latch Design with Complete Double Node Upset Tolerant Capability Using C-element *Y. Yamamoto and K. Namba* (Chiba Un.)

12:00—01:00pm Lunch Break

01:00—2:30pm Session 2—Testing *Chair: K. Namba* (Chiba Un.)

- Improving the Resolution of Multiple Defect Diagnosis by Removing and Selecting Tests (Best Paper Award Nominee) *N. Wang, I. Pomeranz, B. Benware, M. E. Amyeen, and S. Venkataraman* (Purdue Un., Mentor Graphics, Intel Corp.)
- A Method to Model Statistical Path Delays for Accurate Defect Coverage *P. K. Javvaji and S. Tragoudas* (So. Illinois Un. Carbondale)
- Investigation of Mean-Error Metrics for Testing Approximate Integrated Circuits *M. Traiola, A. Virazel, P. Girard, M. Barbareschi, and A. Bosio* (Un. Montpellier, Un. Naples Federico II)

02:30—03:00pm Coffee Break

03:00—04:00pm Invited Talk #1: Are System Level Tests Unavoidable for High End Processors? *A. Singh* (Auburn Un.)

04:00—05:00pm Session 3—Devices and Testing (Short Presentations)

- FPGA SEE Test with Ultra-high Energy Heavy Ions *G. Furano, A. Tavoularis, L. Santos, V. Ferlet-Cavrois, C. Boatella, R. G. Alia, P. F. Martinez, M. Kastriotou, V. Wyrwoll, S. Danzeca, M. Tali, D. Gacnik, I. Kramberger, K. Maragos, and G. Lentaris* (ESA/ESTEC, CERN, Skylabs, Un. Maribor, LuxSpace Sarl, NTUA)
- Analysis of Single Event Upsets Based on Digital Cameras with Very Small Pixels *G. H. Chapman, R. Thomas, K. J. C. S. Meneses, I. Koren, and Z. Koren* (Simon Fraser Un., UMASS Amherst)
- MATS**: An On-Line Testing Approach for Reconfigurable Embedded Memories *L. Bozzoli and L. Sterpone* (Polit. di Torino)
- 45 nm Bit-Interleaving Differential 10T Low Leakage FinFET based SRAM with Column-wise Write Access Control *V. Gupta, S. Khandelwal, J. Mathew, and M. Ottavi* (Un. Rome, ITM Un., IIT Patna)

Tuesday, October 9, 2018

09:00—10:00am Keynote #2: Supercomputer Reliability—Actionable Insights from Neutrons, Data Analytics, and Field Data *N. DeBardeleben* (LANL)

10:00—10:30am Coffee Break

10:30—12:00pm Session 4—Programmable Logic and CMOS Technologies *Chair: L. Bozzoli* (Polit. di Torino)

- Threshold Voltage Extraction Using Static NBTI Aging *P. Savanur and S. Tragoudas* (So. Illinois Un. Carbondale)
- Effects of Voltage and Temperature Variations on the Electrical Masking Capability of Sub-65 nm Combinational Logic Circuits *S. Olowogemo, W. Robinson, and D. Limbrick* (Vanderbilt Un., NC A&T State Un.)
- A Placement-aware Soft Error Rate Estimation of Combinational Circuits for Multiple Transient Faults in CMOS Technology *G. I. Paliaroutis, P. Tsoumanis, N. Evmorfopoulos, G. Dimitriou, and G. I. Stamoulis* (Un. Thessaly)

12:00—01:30pm Lunch Break

01:30—2:30pm Invited Talk #2: Detecting and Counteracting Benign Faults and Malicious Attacks in Cyber Physical Systems *I. Koren* (UMASS Amherst)

02:30—03:00pm Coffee Break

03:00—04:30pm Session 5—Aging and Test *Chair: G. Chapman* (Simon Fraser Un.)

- Performance-based and Aging-aware Resource Allocation for Concurrent GPU Applications *Z. Tasoulas, R. Guss, and I. Anagnostopoulos* (So. Illinois Un. Carbondale)
- Multiple Fault Detection in Nano Programmable Logic Arrays *F. Lombardi and P. Junsangsri* (Northeastern Un.)
- Analysis of the Effects of Single Event Upsets (SEUs) on User Memory in FPGA Implemented Viterbi Decoders *Z. Gao, L. Yan, J. Zhu, R. Han, and P. Reviriego* (Tianjin Un., Antonio de Nebrija)

04:30—05:15pm Panel: Radiation Effect

Panelists: *C. Lam* (Sandia NL)
A. Watkins (Blue Origin)
N. DeBardeleben (LANL)
M. Rovatti (European Space Agency)

05:15—06:00pm Reception

06:00—09:00pm Banquet

Wednesday, October 10, 2018

08:30-09:00am Invited Talk #3: Towards Modeling and Simulation of System-level Radiation Effects *C. Lam* (Sandia NL)

09:00—10:00am Session 6—System Level Techniques (Short Presentations) *Chair: S. Jian* (Virginia Tech.)

- Evaluating the Resilience of Parallel Applications *M. Wikening, F. Previlon, D. R. Kaeli, S. Gurumurthi, S. Raasch, and V. Sridharan* (Harvard Un., Northeastern Un., Advanced Micro Devices)
- State Recovery for Coarse-grain TMR Designs in FPGAs Using Partial Reconfiguration *M. Schutz, A. Steininger, F. Huemer, and J. Lechner* (RUAG Space GmbH, TU Wien)
- Hybrid On-line Self-test Strategy for Dual-core Lockstep Processors *A. Floridia and E. Sanchez* (Polit. di Torino)
- Postprocessing Procedure for Reducing the Faulty Switching Activity of a Low-power Test Set *I. Pomeranz* (Purdue Un.)

10:00—10:15am Coffee Break

10:15—11:45am Session 7—Networks, Coding, and Security

- Efficient Non-binary Hamming Codes for Limited Magnitude Errors in MLC PCMs (Best Paper Award Nominee) *A. Das and N. A. Touba* (Un. Texas)
- A Runtime Fault-tolerant Routing Scheme for Partially Connected 3D Networks-on-chip *A. Coelho, A. Charif, N. Zergainoh, and R. Velazco* (Un. Grenoble Alpes)
- Fast Dynamic Device Authentication Based on Lorenz Chaotic Systems *L. Bu, H. Cheng, and M. A. Kinsy* (Heilongjiang Un., Boston Un.)

11:45—12:00pm Closing Remarks and Best Paper Award Presentation