Wednesday October 2 @ ESA-ESTEC

8:00 – 9:00am **Breakfast and Registration**

9:00 – 9:30am **Opening Address**

Dependable Electronics systems in space, ESA's view by *Dr. Riccardo De Gaudenzi, ESA*

9:30 – 10:30am **Keynote #1**

RowHammer and Beyond by *Onur Mutlu, ETH Zurich*

10:30 – 10:45am **Coffee Break**

10:45 – 12:00pm **Session #1: Accelerators**

Chair: Said Hamdioui, TU Delft

S1-1 Reliability Evaluation of Polyphase-filter based Decimators implemented on SRAM-FPGA
Z. Gao, L. Yan, T. Yan and P. Reviriego

S1-2 Scatter Scrubbing: A Method to Reduce SEU Repair Time in FPGA Configuration Memory
M. Mousavi, H. R. Pourshaghaghi, A. Kumar and H. Corporaal

S1-3 Efficient Error-Tolerant Quantized Neural Network Accelerators ☆
G. Gambardella, J. Kappauf, M. Blott, C.Doehring, M. Kumm, P. Zipf and K. Vissers

12:00 – 1:00pm **Special Session #1: Rebooting Computing**

SS1-1 Organisers: A. Bosio, I. Vatajelu, S.Hamdioui
Chair: Luigi Dilillo, LIRMM

Rebooting Computing: The Challenges for Test and Reliability
A. Bosio, I. O'Connor, G. Rodrigues, F. Lima, E.I. Vatajelu, G. Di Natale, L. Anghel, S.Nagarajan, M. Fieback and S. Hamdioui

1:00 – 2:00pm **Lunch**

2:00 – 3:45pm **Session #2: Testing and fault tolerance**

Chair: Alberto Bosio, University of Lyon

S2-1 State Encoding with Stochastic Numbers for Transient Fault Tolerant Linear Finite State Machines ☆
H. Ichihara, Y. Maeda, T. Iwagaki and T. Inoue

S2-2 Analog Test Interface for IEEE 1687 Employing Split SAR Architecture to Support Embedded Instrument Dependability Applications
J. Pathrose, L. van de Logt and H. Kerkhoff

S2-3 Detecting SEUs in Noisy Digital Imagers with small pixels
K. J. Coelho Silva Menes, G. H. Chapman, R.Thomas, I. Koren and Z. Koren

S2-4 A Low Capture Power Oriented X-filling Method Using Partial MaxSAT Iteratively
T. Hosokawa, K. Misawa, Y. Hirama, H.Yamazaki, M. Yoshimura and M. Arai

3:45 – 4:15pm **Coffee Break**

4:15 – 5:30pm **Session #3: GPUs**

Chair: Giorgio Di Natale, TIMA – CNRS

S3-1 Understanding of GPU Architectural Vulnerability for Deep Learning Workloads
D. Santoso and H. Jeon

S3-2 Combining Cluster Sampling and ACE analysis to improve fault-injection based reliability evaluation of GPU-based systems
A. Vallero and S. Di Carlo

S3-3 A Comprehensive Evaluation of the Effects of Input Data on the Resilience of GPU Applications
F. G. Previlon, C. Kalra, P. Rech and D. Kaeli

5:30pm **Welcome Cocktails**

Thursday October 3 @ ESA-ESTEC

8:30 – 9:30am **Breakfast and Registration**

9:30 – 10:30am **Keynote #2**

Challenges in AI/ML for safety critical systems by *Riccardo Mariani, NVIDIA*

10:30 – 10:45am **Coffee Break**

10:45 – 12:00pm **Session #4: Parallel Processing**

Chair: Antonio Miele, Politecnico di Milano

S4-1 Simulating wear-out effects of asymmetric multicores at the architecture level
N. Foutris, C. Kotselidis and M. Lujan

S4-2 A Fault-Tolerant MPSoC For CubeSats
C. M. Fuchs, P. Chou, X. Wen, N. M. Murillo, G. Furano, S. Holst, A. Tavoularis, S.-K. Lu, A.Plaat and K. Marinis

S4-3 Increasing the Efficiency and Efficacy of Selective-Hardening for Parallel Applications
D.A. Gonçalves De Oliveira, P. Navaux, P. Rech

12:00 – 1:00pm **Poster Session**

Chair: Dr. Stefano Speretta, TU Delft

P-1 Parity-Based Concurrent Error Detection Schemes for the ChaCha Stream Cipher
A. Zeh, M. Meier, and V. Rieger

P-2 Low Redundancy Double Error Correction Spotty Codes Combined with Gray Coding for 64 Data Bits Memories of 4-bit Multilevel Cell
S. Liu, P. Reviriego, K. Namba, S. Pontarelli, L.Xiao and F. Lombardi

P-3 Protecting Large Word Size Memories against MCUs with 3-bit Burst Error Correction
J. Li, P. Revriiego, L. Xiao and A. Klockmann

P-4 A State Assignment Method to Improve Transition Fault Coverage for Controllers
M. Yoshimura, Y. Takeuchi, H. Yamazaki and T. Hosokawa

P-5 Developing a Configurable Fault Tolerant Multicore System for Optimized Sensor Processing
M. Ulbricht, R. T. Syed and M. Krstic

P-6 Evaluation of TMR effectiveness for soft error mitigation in SHyLoC compression IP implemented on Zynq SoC under heavy ion radiation
A. J. Sánchez-Clemente, Y. Barrios, L. Santos and R. Sarmiento

P-7 CORE-VR: A Coherence and Reusability Aware Low Voltage Fault Tolerant Cache in Multicore
A. Choudhury and B. K. Sikdar

P-8 On the Criticality of Caches in Fault-Tolerant Processors for Space
S. Di Mascio, A. Menicucci, G. Furano and C.Monteleone

P-9 On the Reliability of Convolutional Neural Network Implementation on SRAM-based FPGA
B. Du, S. Azimi, C. De Sio, L. Bozzoli and L.Sterpone

1.00 - 2.00pm **Lunch**

2.00 – 2.45pm **Poster Session, continue**

2.45 – 3.15pm **Coffee Break**

3:15 – 4:30pm **Session #5: Security and Verification**

Chair: P. Reviriego, Univ. Carlos III de Madrid

S5-1 Preventing Scan Attack through Test Response Encryption
S. Ahlawat, J. Tudu, M.S. Gaur, M. Fujita, and V. Singh

S5-2 Co-relation Scan Attack Analysis (COSAA) on AES: A Comprehensive Approach
D. Ray, S. Singh, S. S. Ali and S. Biswas

S5-3 Protecting RSA Hardware Accelerators against Differential Fault Analysis through Residue Checking
A. Lasheras, R. Canal, E. Rodríguez and L.Cassano

5:00 – 10:00pm **Social Event and Dinner**

Friday October 4 @ TU Delft

8:30 – 9:30am **Breakfast and Registration**

9:30 – 10:30am **Keynote #3**

From Cross-Layer Resilience for On-Chip Systems to Robust Machine Learning by
Muhammad Shafique, TU Wien

10:30 – 10:45am **Coffee Break**

10:45 – 12:00pm **Session #6: Memories**

Chair: Adrian Evans, CEA LETI

S6-1 High Performance Memory Repair ☆
F. Merchant, A. Devarajan, A. Basu, D. Ashen, B. Yelton and P. Joshi

S6-2 Predicting Single Event Upsets in DRAM
D. Kline Jr, S. Longofono, R. Melhem, A.Jones

S6-3 Scalable and Configurable Multi-Chip SRAM in a Package for Space Applications
A. Simevski, P. Skoncej, C. Calligaro, M.Krstic

12:00 – 1:00pm **Lunch**

1:00 – 2:00pm **Special Session #2: Autonomous Systems**

Organisers: M. Jenihhin, Matteo S. Reorda
Chair: Paolo Rech, LANL / UFRGS

SS2-1 Challenges of Reliability Assessment and Enhancement in Autonomous Systems
M. Jenihhin, M. S. Reorda, A. Balakrishnan and D. Alexandrescu

SS2-2 On-line Testing for Autonomous Systems driven by RISC-V Processor Design Verification
A. Ruospo, R. Cantoro, E. Sanchez, P. D. Schiavone, A. Garofalo and L. Benini

SS2-3 HYPERSDF: a highly reliable platform for data fusion in autonomous driving applications
M. Violante, L. Bongiovanni, R. Groppo and P. Santero

2:00 – 3:15pm **Session #7: Memories**

Chair: Prashant Joshi, Intel

S7-1 Effects of Heavy Ion and Proton Irradiation on a SLC NAND Flash Memory
L. M. Luza, A. Bosser, V. Gupta, A. Javanainen, A. Mohammadzadeh and L. Dilillo

S7-2 Fault tolerant photovoltaic array: a repair circuit based on memristor sensing
L. Gnoli, G. Carnicelli, A. Parisi, U. Luca, S. I. P. Ibarra, B. Kabashi, F. Michieletti, M. Graziano, M. Vacca, M. Jimson and M. Ottavi

S7-3 Testing of In-Memory-Computing 8T SRAMs
T.-L. Tsai, J.-F. Li, C.-L. Hsu and C.-T. Sun

3:15 – 3:30pm **Closing Remarks**

3:30pm **Drinks**

Best paper candidate: ☆

Program of the 32th IEEE Int. Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

ESA-ESTEC & TU Delft, The Netherlands

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