IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

October 8th - 10th, 2024, Harwell, Oxfordshire, UK

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Call for Papers.

DFT is an annual Symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies, RISC-V architectures and AI-based solutions. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, availability, and security that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following:

1. **Yield Analysis and Modeling:** Defect/fault analysis and models; statistical yield modeling; diagnosis; critical area and other metrics.
2. **Testing Techniques:** Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; online testing; signal and clock integrity.
3. **Design for Testability in IC Design:** FPGA, SoC, NoC, ASIC, low power design and micro-processors, including RISC-V architectures.
4. **Error Detection, Correction, and Recovery:** Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques; architectural and system-level techniques.
5. **Dependability Analysis and Validation:** Fault injection techniques and frameworks; dependability and characterization, cross-layer reliability analysis, dependability analysis for AI and machine learning.
6. **Repair, Restructuring and Reconfiguration:** Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing; reliable FPGA systems.
7. **Defect and Fault Tolerance:** Reliable circuit/system synthesis; fault tolerant design; design space exploration for dependable systems, transient/soft faults.
8. **Radiation effects:** SEEs on nanotechnologies; modeling of radiation environments; radiation experiments; radiation hardening techniques.
9. **Aging and Lifetime Reliability:** Aging characterization and modeling; design and run-time reliability, thermal, and variability management and recovery.
10. **Dependable Applications and Case Studies:** Methodologies and case studies: 2.5D/3D ICs, IoT, automotive/railway/avionics/space, autonomous systems, industrial control, fail-safe systems, dependable AI.
11. **Emerging Technologies:** Error management techniques for quantum computing, memristors, spintronics, microfluidics, approximate computing, etc.
12. **Design for Security:** Fault attacks, fault tolerance-based countermeasures, scan-based attacks and countermeasures, hardware trojans, system obfuscation and logic locking, secure AI, security vs. reliability, interaction between VLSI test, trust, and reliability.

Paper Submission: Authors are invited to submit original and unpublished contributions in the areas described above. Authors must first submit a one paragraph abstract, followed by the final paper for review. Submitted papers should be no longer than 6 pages and adhere to the IEEE conference template, 2-columns style (available on conference web site). Papers can be accepted as regular papers (former oral presentations) or short papers (formerly posters). Both types of paper will be included in the IEEE proceedings. The page limit for proceedings is 6 pages for regular papers and 4 pages for short papers. Authors of a 6 page submission accepted as a short paper must reduce it to 4 pages, for publication. Full paper versions of relevant work presented, or under submission, for the RISC-V Summit are welcome. Please refer to the symposium web page for updated information.

Call for Special Sessions: Proposals for Special Sessions are also invited. For more information, visit symposium website and see the specific call.

Paper Publication: Only original, unpublished work will be accepted, for oral presentation at the symposium. Proceedings will be published by the IEEE Computer Society and will appear in the Digital Library

Author Registration: Every accepted paper MUST have at least one *full* paid registration by the time the camera-ready paper is submitted for inclusion in the proceedings, and one of the authors MUST attend the Symposium and present the paper.

Best Paper Award: The committee will select a best paper award and best student paper awards which will be attributed at the conference.

Journal Special Issue associated with the conference: Authors of accepted papers at DFTS 2024 will be invited to submit an extended version of the work to a special issue of an area journal dedicated to the conference 2024 edition.

Prospective authors should adhere to the following deadlines:

Abstract submission:	~~**Apr 26**~~ **May 10, 2024**
Full paper submissions:	~~**May 3**~~ **May 17, 2024**
Notification of acceptance:	**July 8, 2024**
Camera ready and author's registration:	**July 22, 2024**

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DFT 2024 webpage: http://www.dfts.org